# On Theory and Performance of Solid-State Microwave Distributed Amplifiers

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*Abstract* — **The performance characteristics of $n$-link distributed amplifiers employing GaAs MESFET's are studied. At first, formulas of the symmetrical amplifier using lumped circuit elements are developed for the case of an idealized FET model. The theoretical analysis is then extended to distributed line elements and later to an $S$-parameter derived transistor model. In efforts to optimize amplifier performance, the restriction of circuit symmetry is subsequently removed and the performance characteristics of two concepts, that of equal characteristic impedances and that of equal line lengths, are proposed and compared.**

**Based on this analysis and practical considerations, several three-link hybrid amplifiers utilizing the equal line lengths approach have been assembled and test results are reported. A gain of $G = 5.5 \pm 0.6$ dB was measured over the bandwidth of 2–20 GHz. Across this frequency band a maximum VSWR of 2.2:1 for the input and 2.5:1 for the output terminal have been realized, while a minimum output power at the 1-dB compression points of 19.3 dBm was achieved from 2–18 GHz. Agreement between measured and computed small-signal gain as well as reverse isolation is excellent.**

## I. INTRODUCTION

THE PRINCIPLE of the distributed amplifier was first proposed by W. S. Percival in 1935 [1]. However, Percival's invention did not go into widespread active use until after E. L. Ginzton *et al.* published their analysis of the distributed amplifier in 1948 [2]. First experimental results verifying the theoretical predictions were reported shortly thereafter [3], [4] and a more detailed mathematical theory using matrix algebra followed in 1953 [5].

The new concept was based on the idea to separate the interelectrode capacitances of the active components (electron tubes at the time) by means of artificial transmission lines, while adding their transconductances. As a result, it was possible to obtain amplification over much wider bandwidths than was achievable with conventional amplifier systems.

In pursuit of larger gain-bandwidth products and more severe rise-time requirements, the distributed amplifier concept has lately been successfully applied to monolithic GaAs MESFET amplifiers at microwave frequencies [6]–[8]. Recently Ayasli *et al.*, in a detailed description of their 1–13-GHz monolithic amplifier, have published design formulas for the gain of a traveling-wave amplifier based on an approach that approximates gain and drain lines as continuous structures [9]. Similarly, J. B. Beyer *et al.* developed a closed-form expression for the gain that depends on the circuit's propagation constants and the gate circuit cutoff frequency [10]. It is the purpose of this paper to contribute to the theoretical analysis and the practical design of GaAs MESFET distributed amplifiers. The theoretical study is initially conducted by means of a simple transistor model employed in an amplifier with either artificial or real transmission lines. This effort is then extended to a much more sophisticated model of a transistor developed from its measured $S$-parameters. In contrast to the continuous structure approach adopted by several authors [9], [11], [12], the analysis of this paper is based on employing a finite number of active and passive circuit elements. Based on the understanding of the electrical behavior gained in the analysis, two versions of a three-link distributed amplifier are studied with the aid of a computer. Both employ real transmission lines and contain a simple input matching network. The first version makes use of transmission lines with identical characteristic impedances and different line lengths between transistors on the drain and the gate side. The second version is based on equal line lengths between transistors and different characteristic impedances. Both designs are optimized for best broad-band performance.

The latter approach is then chosen for the final design of an $S$–$Ku$-band amplifier module because of practical considerations. Measured results prove the feasibility of the GaAs MESFET distributed amplifier principle for multioctave microwave amplification. The concept's ability to add the transconductances of $n$ transistors while separating their capacitive parasitics makes it possible to achieve extremely wide bandwidths up to very high frequencies with effectively very wide gates. The latter obviously has a beneficial impact on the amplifier's power handling capabilities.

## II. THEORETICAL ANALYSIS

### A. Elementary Circuit

The elementary circuit or link of a lumped element distributed amplifier can be represented by a four-port as shown in the schematic of Fig. 1(a). Replacing the transistor of Fig. 1(a) by its two-port representation with the current source $i_k$ leads to the equivalent circuit shown in Fig. 1(b). The voltages and currents of the individual ports

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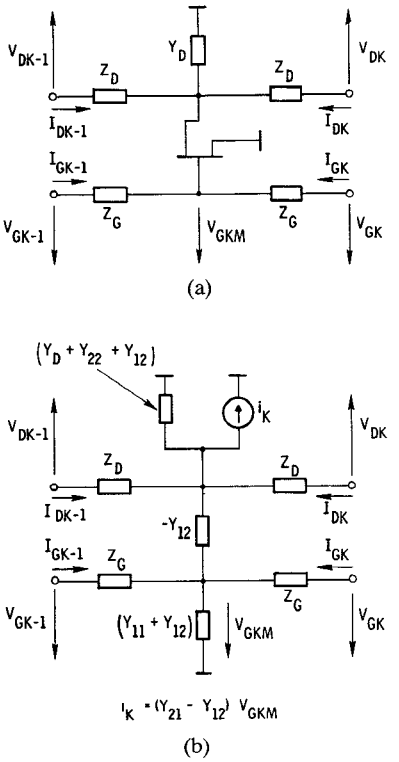


Fig. 1. Circuit topology of the basic link of a nonsymmetric distributed amplifier using lumped circuit elements.

and their relation to each other may be determined with the matrix equation

$$\begin{bmatrix} V_{Dk-1} \\ I_{Dk-1} \\ V_{Gk-1} \\ I_{Gk-1} \end{bmatrix} = \left[\begin{array}{c|c} C_{11} & C_{12} \\ \hline C_{21} & C_{22} \end{array}\right] \begin{bmatrix} V_{Dk} \\ -I_{Dk} \\ V_{Gk} \\ -I_{Gk} \end{bmatrix} = A \begin{bmatrix} V_{Dk} \\ -I_{Dk} \\ V_{Gk} \\ -I_{Gk} \end{bmatrix} \tag{1}$$

where for lumped elements

$$C_{11} = \begin{bmatrix} [1+Z_D(Y_D+Y_{22})] & Z_D[2+Z_D(Y_D+Y_{22})] \\ (Y_D+Y_{22}) & [1+Z_D(Y_D+Y_{22})] \end{bmatrix} \tag{1a}$$

$$C_{12} = Y_{21}\begin{bmatrix} Z_D & Z_GZ_D \\ 1 & Z_G \end{bmatrix} \tag{1b}$$

$$C_{21} = Y_{12}\begin{bmatrix} Z_G & Z_GZ_D \\ 1 & Z_D \end{bmatrix} \tag{1c}$$

$$C_{22} = \begin{bmatrix} (1+Z_GY_{11}) & Z_G(2+Z_GY_{11}) \\ Y_{11} & (1+Z_GY_{11}) \end{bmatrix}. \tag{1d}$$

The matrix $[A]$ of (1) can also be written in the form

$$A = A_1A_2A_1 \tag{2}$$

which makes it more convenient to use if one decides to replace the lumped elements $Z_G$ and $Z_D$ of Fig. 1 with transmission line elements of the characteristic impedances $Z_G$ and $Z_D$ and the electrical lengths of $\frac{1}{2}\theta_G$ and $\frac{1}{2}\theta_D$. In this case, the transistor and the admittance $Y_D$ are represented by

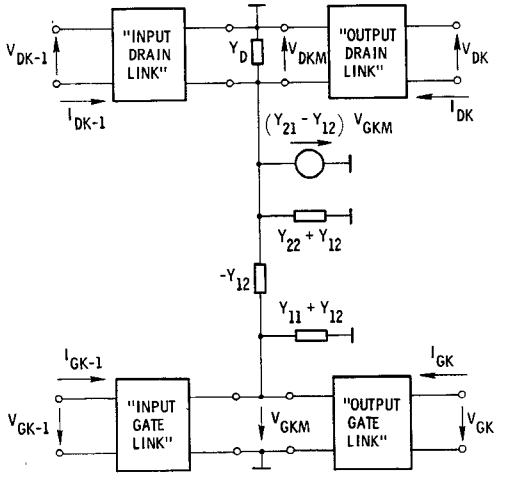


Fig. 2. Equivalent four-port representation of the basic link in its general form.

$$A_2 = \begin{bmatrix} 1 & 0 & 0 & 0 \\ (Y_D+Y_{22}) & 1 & Y_{21} & 0 \\ 0 & 0 & 1 & 0 \\ Y_{12} & 0 & Y_{11} & 1 \end{bmatrix} \tag{2a}$$

while the remaining circuit is characterized by

$$A_1 = \begin{bmatrix} 1 & Z_D & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & Z_G \\ 0 & 0 & 0 & 1 \end{bmatrix} \tag{2b}$$

when lumped elements, and by

$$A_1 = \begin{bmatrix} \cos\frac{\theta_D}{2} & jZ_D\sin\frac{\theta_D}{2} & 0 & 0 \\ j\frac{1}{Z_D}\sin\frac{\theta_D}{2} & \cos\frac{\theta_D}{2} & 0 & 0 \\ 0 & 0 & \cos\frac{\theta_G}{2} & jZ_G\sin\frac{\theta_G}{2} \\ 0 & 0 & j\frac{1}{Z_G}\sin\frac{\theta_G}{2} & \cos\frac{\theta_G}{2} \end{bmatrix} \tag{2c}$$

when transmission line elements are being employed.

For the general case that the linking elements are neither identical nor symmetrical, the matrix equation (1) takes the form

$$\begin{bmatrix} V_{Dk-1} \\ I_{Dk-1} \\ V_{Gk-1} \\ I_{Gk-1} \end{bmatrix} = A_k \begin{bmatrix} V_{Dk} \\ -I_{Dk} \\ V_{Gk} \\ -I_{Gk} \end{bmatrix} \tag{3}$$

where

$$A_k = A_{1k}A_{Fk}A_{2k}. \tag{3a}$$

$[A_{1k}]$ is the matrix of the input link and $[A_{2k}]$ is that of the output link as shown in Fig. 2, while $[A_{Fk}]$ consitutes the

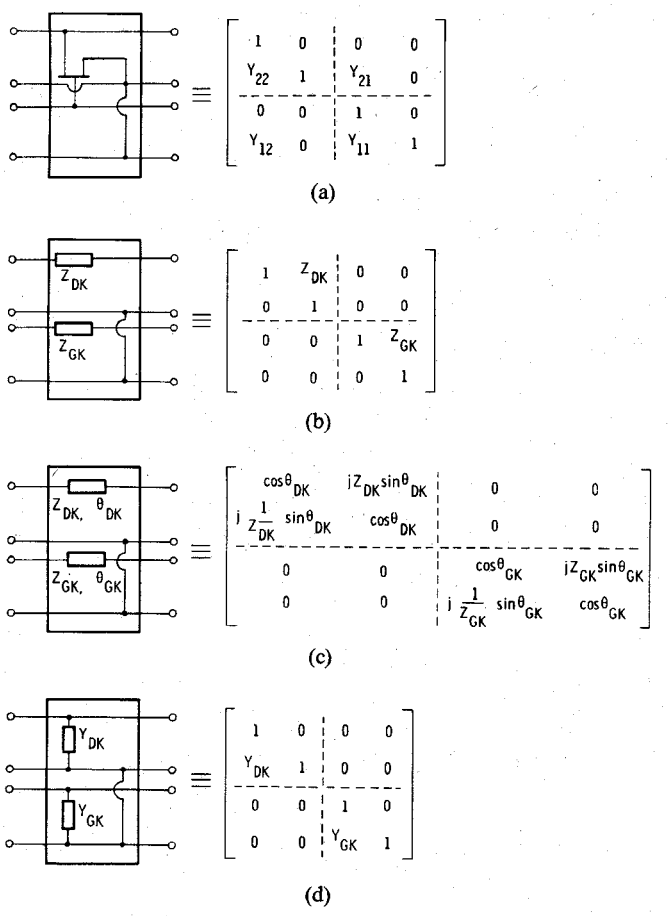


Fig. 3. Transformation matrices of the four-ports typically employed in distributed amplifier design.

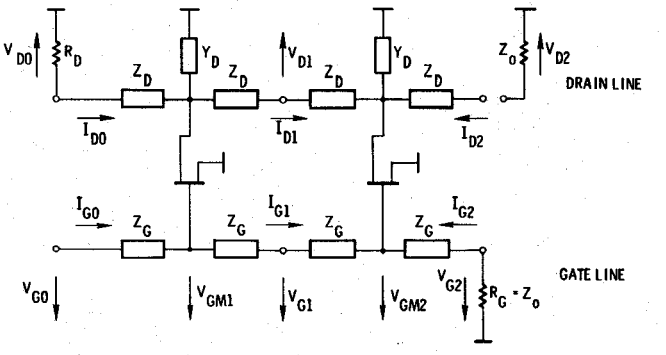


Fig. 4. Schematic of a distributed amplifier consisting of two symmetric links employing lumped elements.

MESFET's chain matrix. The latter is contained in Fig. 3 along with the matrices of several other four-ports that are typically used in distributed amplifier design.

Formulating the boundary conditions in accordance with the currents and voltages chosen in the schematic of the two-link module shown in Fig. 4 we obtain

$$V_{D0} + R_D I_{D0} = 0 \tag{4a}$$

and

$$V_{G2} + R_G I_{G2} = 0. \tag{4b}$$

Hence, cascading $n$-links and terminating the idle ports with $R_G$ and $R_D$ yields the matrix equation

$$\begin{bmatrix} V_{D0} \\ -R_D^{-1}V_{D0} \\ V_{G0} \\ I_{G0} \end{bmatrix} = D \begin{bmatrix} V_{Dn} \\ -I_{Dn} \\ V_{Gn} \\ R_G^{-1}V_{Gn} \end{bmatrix} \tag{5}$$

where for arbitrary links

$$D = \prod_{k=0}^{n} A_k \tag{5a}$$

and for identical links

$$D = A^n. \tag{5b}$$

The insertion gain of the amplifier can now be determined as a function of the matrix elements of (5). After some algebraic steps we obtain

$$\text{Gain} = \left| 2Y_0 \frac{C_2}{C} \right|^2 \tag{6}$$

with

$$C_1 = D_{43} + R_G^{-1}D_{44} + Y_0\left(D_{33} + R_G^{-1}D_{34}\right) \tag{6a}$$

$$C_2 = D_{23} + R_G^{-1}D_{24} + R_D^{-1}\left(D_{13} + R_G^{-1}D_{14}\right) \tag{6b}$$

$$C = C_1\left[D_{21} + Y_0 D_{22} + R_D^{-1}(D_{11} + Y_0 D_{12})\right] - C_2\left[D_{41} + Y_0 D_{42} + Y_0(D_{31} + Y_0 D_{32})\right]. \tag{6c}$$

Equation (6) represents the exact solution for the insertion gain of a distributed amplifier module in its most general form. In our initial analysis, however, we will neglect the influence of feedback ($Y_{12} = 0$), choose identical elements for the gate and the drain line, i.e., $Y_{11} = Y_D + Y_{22} = Y_S$ and $Z_G = Z_D = Z_L$, and replace the active elements with the idealized equivalent circuit of Fig. 5(c).

### *B. Amplifier with Simple Transistor Model*

The elementary circuit of a highly simplified link of the distributed amplifier is shown in Fig. 5(a) while Fig. 5(c) presents the idealized topology of the amplifier's active element consisting of the current source $i_K$ and the capacitances $C_{gs} = C$ and $C_{ds}$. In the following analysis, the lumped circuit elements of the basic distributed amplifier are represented by

$$Z_L = j\omega\frac{L}{2} \tag{7a}$$

$$Y_S = j\omega C = j\omega C_{gs} = j\omega(C_{ds} + C_D) \tag{7b}$$

$$R_G = R_D = Z_0 = \sqrt{\frac{L}{C}}. \tag{7c}$$

The transconductance of the MESFET is approximated by

$$Y_{21} \cong g_m \tag{8}$$

while the drain capacitance added for circuit symmetry is represented by $C_D$ (7b). Replacing a GaAs MESFET by the three-element circuit of Fig. 5(c) is obviously an over-simplification that may result in significant errors when

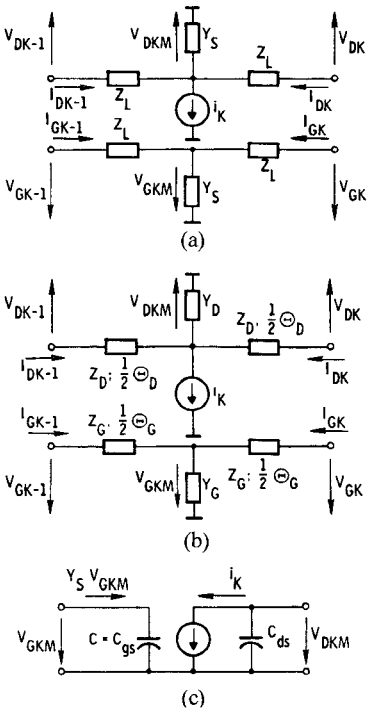


Fig. 5. Circuit topology of the basic link of a symmetric distributed amplifier using (a) lumped elements, (b) transmission line elements, and (c) an idealized active device model.

calculating the amplifier's performance characteristics at microwave frequencies. However, in the interest of arriving at "relatively simple" analytic expressions for the amplifier's gain and VSWR performance, we have restricted the analysis in this section to the active device model as shown in Fig. 5(c).

Applying (5) to the circuit topology of Fig. 5(a) and cascading $n$-links, one easily arrives at the voltages and currents of the $n$-link amplifier

$$\begin{bmatrix} V_{D0} \\ -R_D^{-1}V_{D0} \\ V_{G0} \\ I_{G0} \end{bmatrix} = \left[\begin{array}{c|c} C_{11} & C_{12} \\ \hline C_{21} & C_{22} \end{array}\right]^n \begin{bmatrix} V_{Dn} \\ -I_{Dn} \\ V_{Gn} \\ R_G^{-1}V_{Gn} \end{bmatrix}. \tag{9}$$

After defining the normalized frequency

$$\Omega = \frac{\omega}{\omega_0} = \omega\sqrt{LC} \tag{10}$$

its submatrices can readily be expressed as a function of $\Omega$ using (7) and (8)

$$C_{11} = C_{22} = \begin{bmatrix} \left(1-\frac{1}{2}\Omega^2\right) & j\frac{Z_0}{2}\Omega\left(2-\frac{1}{2}\Omega^2\right) \\ jY_0\Omega & \left(1-\frac{1}{2}\Omega^2\right) \end{bmatrix} \tag{11a}$$

$$C_{12} = gm\begin{bmatrix} j\frac{Z_0}{2}\Omega & -\frac{Z_0^2}{4}\Omega^2 \\ 1 & j\frac{Z_0}{2}\Omega \end{bmatrix} \tag{11b}$$

$$C_{21} = [0]. \tag{11c}$$

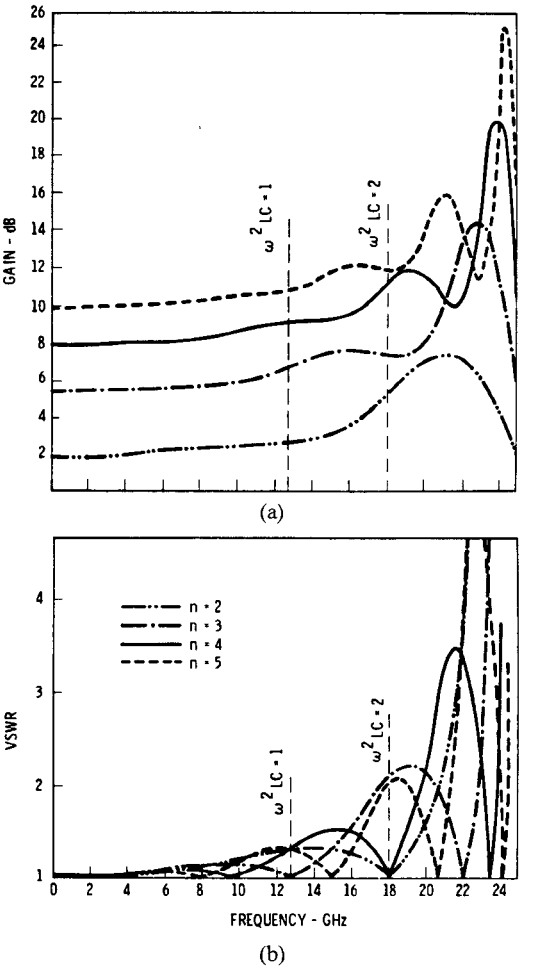


Fig. 6. Computed gain and VSWR of a symmetric distributed amplifier employing $n$ links containing lumped elements. ($C = 0.25$ pF, $L = 0.625$ nH, $gm = 25$ mS, $R_G = R_D = 50\ \Omega$.)

If we now terminate the idle gate port and the idle drain port with $R_G = R_D = Z_0$, then the $S$-parameters of the $n$-link amplifier can be expressed in terms of only the normalized frequency $\Omega$. In case of the two-link module of Fig. 4 we find

$$S_{11} = S_{22} = \frac{-j\frac{1}{4}\Omega^3\left(1-\frac{1}{2}\Omega^2\right)}{\left(1-2\Omega^2+\frac{1}{2}\Omega^4\right)+j\Omega\left(1-\frac{1}{2}\Omega^2\right)\left(2-\frac{1}{4}\Omega^2\right)} \tag{12a}$$

$$S_{12} = 0 \tag{12b}$$

$$S_{21} = -gmZ_0\frac{\left[1-\frac{1}{4}\Omega^2(7-\Omega^2)\right]+j\Omega(2-\Omega^2)}{\left[\left(1-2\Omega^2+\frac{1}{2}\Omega^4\right)+j\Omega\left(1-\frac{1}{2}\Omega^2\right)\left(2-\frac{1}{4}\Omega^2\right)\right]^2}. \tag{12c}$$

It can be seen from (12) that the $S_{21}$-parameter of even the highly idealized two-link distributed amplifier contains terms of the normalized frequency whose exponents are anywhere between 1 and 10. The highest exponential term for the normalized frequency of the three-link module in the formula for $S_{21}$ is $\Omega^{14}$ appearing in the denominator.

The distributed amplifier's gain and input and output VSWR for $n = 2$, 3, 4, and 5 are plotted in Fig. 6. Here the

active device has a transconductance of $g_m = 25$ mS and an input capacitance of $C = 0.25$ pF while the inductivity is $L = 0.625$ nH. This transconductance and capacitance are representative of a GaAs MESFET with a $0.5 \times 300$-$\mu$m gate and a $2 \times 10^{17}$-cm$^{-3}$ carrier concentration, and are typical for a device that our Semiconductor Department fabricates in large quantities. When examining the gain curves of Fig. 6, it becomes apparent that the amplifier's gain variations with frequency are within acceptable levels as long as the condition

$$0 \leqslant \omega^2 LC \leqslant 1 \tag{13}$$

is satisfied. It will be shown in Section II-C that acceptable gain variations within the limits of (13) exist even when the idealized device is replaced by an $S$-parameter derived transistor model. Within the boundaries of (13) the gain is approximately that of the unit at the dc operation, namely

$$G(\Omega = 0) = |S_{21}(\Omega = 0)|^2 = \left(\frac{n}{2} gmZ_0\right)^2. \tag{14}$$

The expression (14) is the well-known formula for the gain of the unattenuated distributed amplifier [9], [10]. However, gain outside the limits of (13) increasingly fluctuates with frequency and takes on a very erratic pattern for

$$\omega^2 LC > 2$$

deviating significantly from (14).

At frequencies at which lumped circuit elements lose their linear frequency dependency it becomes necessary to replace them by distributed line elements. This is especially the case for the lumped inductivities $Z_L$ which, as shown in Fig. 5(b), have been replaced by transmission line elements of the characteristic impedances $Z_G$ and $Z_D$, having the electrical lengths $\frac{1}{2}\theta_G$ and $\frac{1}{2}\theta_D$. Using the circuit topology of Fig. 5(b) the voltages and currents of the $k$th link may be expressed by (1) and (2) when inserting the matrices (2a) for the active element and (2c) for the transmission line elements.

As was the case for the lumped element amplifier, the input and output voltages of the $n$-link module can be determined with (5) and (5b), while the gain may be obtained with (6). Because of the enormous complexity of the resulting formulas, however, no attempt has been made to express the reflection coefficients or the gain of even the simple two-link amplifier in closed form. The computed gain and VSWR's for $Z_G = Z_D$, $\frac{1}{2}\theta_G = \frac{1}{2}\theta_D$, and $R_G = R_D = Z_0$, are plotted in Fig. 7 for $n = 2$, 3, 4, and 5. The amplifiers contain the identical active device model (Fig. 5(c)) employed in case of the distributed amplifier using lumped elements. In addition, the electrical lengths $\frac{1}{2}\theta_G = \frac{1}{2}\theta_D$ were chosen such that identical reflection coefficients for both the amplifier with lumped and with transmission line elements occur at

$$\omega^2 LC = -jZ_{G,D} Y_{G,D} \tan\Theta_{G,D} = 2 \tag{15a}$$

where

$$Y_{G,D} = j\omega C. \tag{15b}$$

Comparing the performance curves of both amplifiers

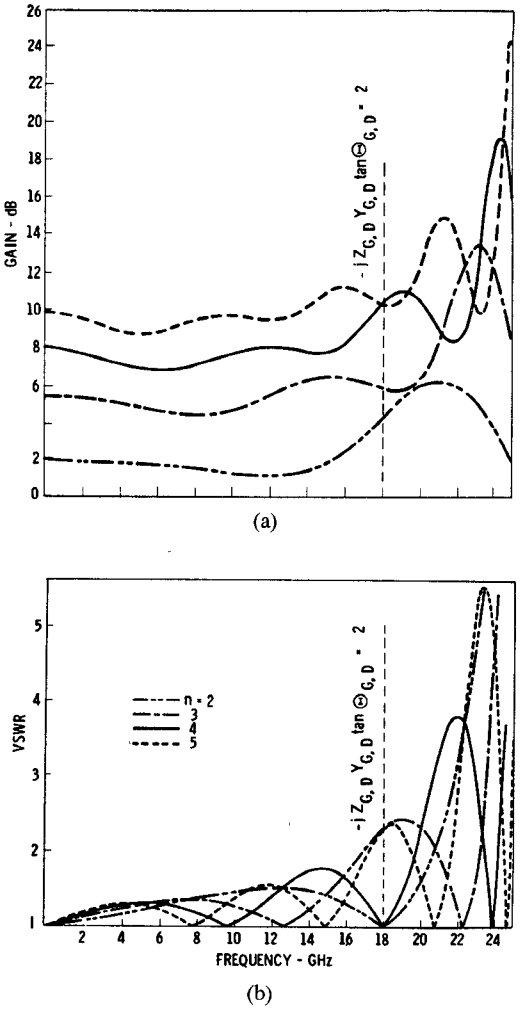


Fig. 7. Computed gain and VSWR of a symmetric distributed amplifier employing $n$-links containing distributed line elements. ($Z_G = Z_D = 125$ Ω, $\theta_G = \theta_D = 32.7°$ @20 GHz, $C_G = 0.25$ pF, $gm = 25$ mS, $R_G = R_D = 50$ Ω.)

(Figs. 6 and 7) reveals that the circuit using lumped elements exhibits slightly better gain and VSWR behavior than its transmission line counterpart. Gains of both versions are the same at low frequencies (14) and identical to that of a lossy match amplifier with the transconductance $ng_m$ and the resistances $R_G = R_D = Z_0$ [13]. The identity that exists between a distributed amplifier and the lossy match amplifier at $\Omega = 0$ will be used in the following section when we attempt to determine the gain of a distributed amplifier that employs a transistor model with a finite drain-to-source resistance $R_{ds}$.

### *C. Amplifier with Transistor Model Based on S-Parameters*

The electrical behavior of an amplifier using a GaAs MESFET may significantly deviate from that incorporating the highly simplified model of Fig. 5(c). It is for this reason that we now extend the analysis to a distributed amplifier that employs a transistor model derived from a GaAs MESFET's $S$-parameters.

Since a GaAs MESFET has a finite resistance between drain and source ($R_{ds}$) the results presented in Figs. 6 and 7 are not applicable at very low frequencies unless the sum

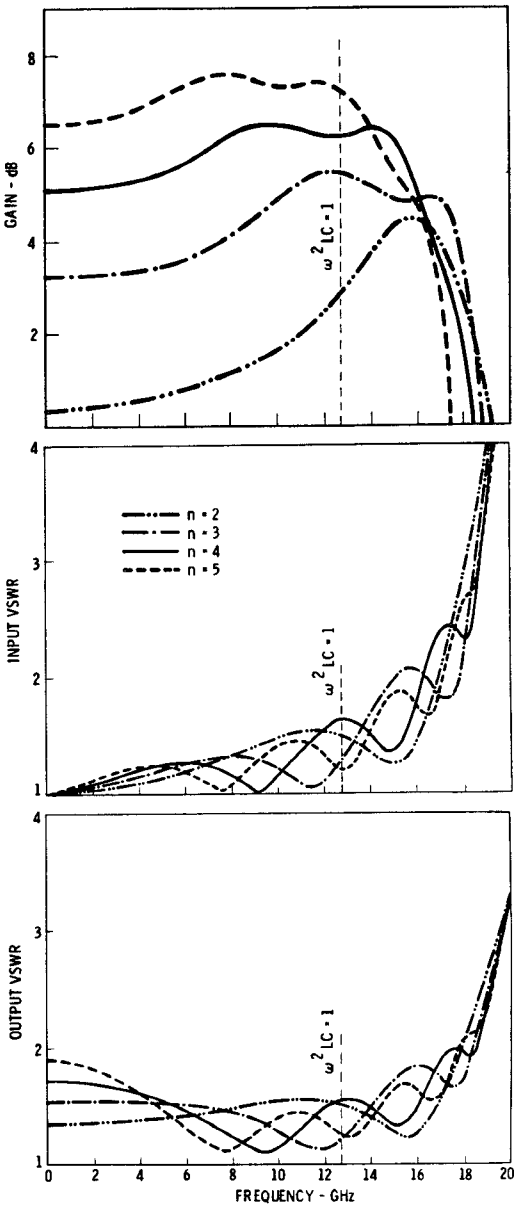


Fig. 8. Computed gain and VSWR of a symmetric distributed amplifier with lumped elements and $S$-parameter derived transistor model. ($L = 0.625$ nH, $C_{ds} + C_D = 0.25$ pF, $R_G = R_D = 50\ \Omega$.)

of the drain–source conductances

$$\sum G_{ds} = nG_{ds} \ll Z_0^{-1}. \tag{16}$$

As indicated earlier, for $\Omega = 0$, the distributed amplifier with $n$ transistors is identical to a lossy match amplifier with the gate conductance ($G_G$), the drain conductance ($G_D + nG_{ds}$), and the transconductance ($ng_m$). The $S$-parameters of the distributed amplifier at low frequencies are therefore approximated by [13]

$$S_{11} \cong \frac{1 - G_G Z_0}{1 + G_G Z_0} \tag{17a}$$

$$S_{12} \cong 0 \tag{17b}$$

$$S_{21} \cong \frac{-2ngmZ_0}{(1 + G_G Z_0)(1 + G_D Z_0 + nG_{ds} Z_0)} \tag{17c}$$

$$S_{22} \cong \frac{1 - (G_D + nG_{ds}) Z_0}{1 + (G_D + nG_{ds}) Z_0}. \tag{17d}$$

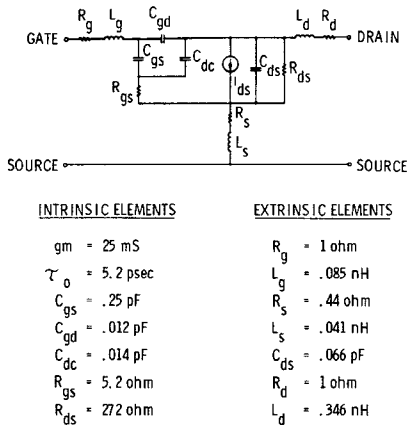


Fig. 9. FET model and its element values.

While the scattering parameters (17) may be used to determine the approximate gain and VSWR's up to frequencies of 1–2 GHz, they may also serve as the starting point for the design of a broad-band distributed amplifier extending its bandwidth to higher frequencies.

We will now compute the gain and the input and output VSWR's of the distributed amplifier incorporating an $S$-parameter derived transistor model. The computations are based on (5), and the resulting curves are plotted in Fig. 8. They are computed for a transistor whose model and element values are presented in Fig. 9. It should be pointed out that the simplified model of Fig. 5(c) and the $S$-parameter derived FET model of Fig. 9 have identical values of those elements that both models have in common, i.e., $g_m = 25$ mS and $C_G = C_{gs} = 0.25$ pF. In addition, the drain capacitance $C_D$ has been chosen so that $C_D + C_{ds} = C_G = C_{gs}$ while the terminations of the idle ports are $R_G = R_D = 50\ \Omega$. The comparison of the characteristics of the lumped element amplifier circuits (Figs. 6 and 8) shows a significant reduction in bandwidth and gain of the distributed amplifier employing the transistor model of Fig. 9 over that incorporating the simplified model of Fig. 5(c). While the finite drain resistor $R_{ds}$ is responsible for the gain reduction at low frequencies, the GaAs MESFET's parasitics limit the bandwidth and the gain at high frequencies, especially $R_{gs}$.

When replacing the lumped elements by sections of transmission lines of relatively high characteristic impedances and in accordance with condition (15), the amplifier's gain and VSWR performance experience only slight changes. The quantitative differences in the performances of the two versions can be determined by comparing the curves of Figs. 8 and 10. As was the case for the simple transistor model, the distributed amplifier using lumped elements exhibits slightly better gain and VSWR characteristics. However, if the desired band extends into $Ku$-band and beyond, the design based on the transmission line seems to be the more appropriate approach.

## III. Design Considerations

So far we have confined the analysis to amplifiers that have identical circuit elements in both the gate and the drain line and, in addition, are terminated with $R_G = R_D =$

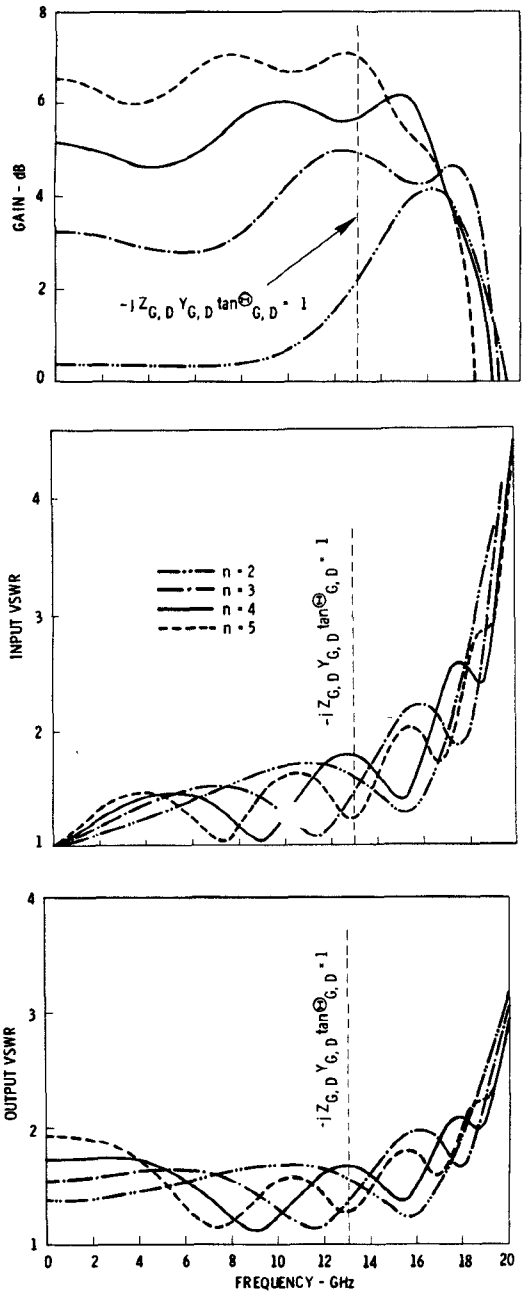


Fig. 10. Computed gain and VSWR of a symmetric distributed amplifier with distributed line elements and $S$-parameter derived transistor model. ($Z_G = Z_D = 125\ \Omega$, $\theta_G = \theta_D = 32.7°$ @20 GHz, $C_{ds} + C_D = 0.25$ pF, $R_G = R_D = 50\ \Omega$.)

$Z_0$ at their idle ports. As demonstrated in Figs. 8 and 10, the resulting performance does not exhibit the gain flatness characteristics suitable for most amplifier applications. However, gain variations versus frequency may be reduced by means of the circuit parameters. For this reason we extend the analysis to amplifiers whose circuit elements can take any values that are practically realizable; in other words, we abandon the concept of circuit symmetry in favor of amplifier performance. Again, (5) represents the relationship between the input and the output quantities. Since it is our goal to cover at least the 2–18-GHz frequency band, the study is limited to the transmission line version of the amplifier. In this chapter we consider two ways that differ in their design approach.

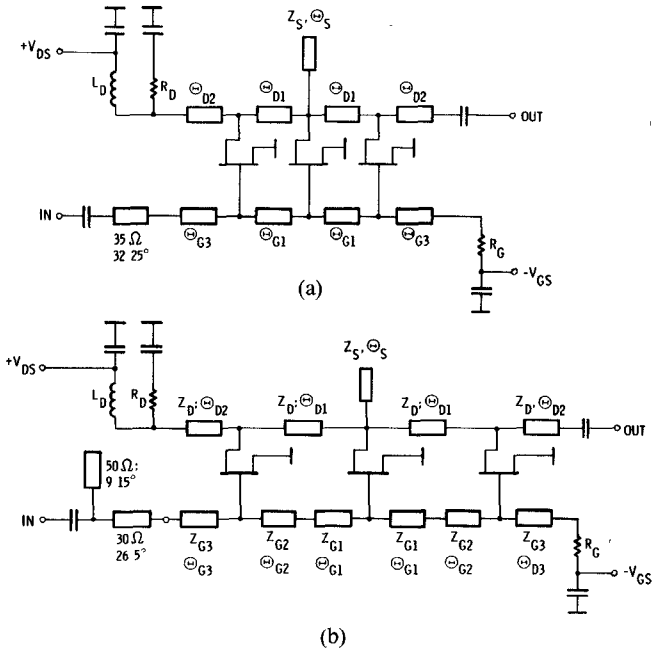


Fig. 11. Schematic of a three-link amplifier (a) with transmission lines of equal impedances or (b) of equal electrical lengths.

### *A. Transmission Lines of Equal Characteristic Impedances*

In the first approach we attempt to optimize the module's performance by varying the electrical lengths $\theta_{Gn}$ and $\theta_{Dn}$ of the transmission line elements for which we elected the same characteristic impedances ($Z_{Gn} = Z_{Dn} = 125\ \Omega$) in both the gate and the drain line. The amplifier's topography is shown in Fig. 11(a). In order to efficiently supply the amplifier module with its drain voltage, a drain inductivity $L_D$ is connected across the idle drain's port. Furthermore, a very simple input matching network is added to improve the unit's input reflection coefficient. Since the inductivity $L_D$ and the input matching network influence the amplifier's performance, they will be included in the optimization routine. The GaAs MESFET itself is represented by the model and its elements described in Fig. 9.

In the following example of a three-link amplifier design whose transistor has a drain–source resistance $R_{ds} = 272\ \Omega$, we start out with the approximation formulas (17). Achieving ideal matching ($S_{11} = S_{22} = 0$) at low frequencies (17) requires $R_G = 50\ \Omega$ and $R_D = 112\ \Omega$. If, as in our case, the transconductance is $g_m = 25$ mS, one calculates with (17c) a low frequency gain of $G = |S_{21}|^2 = 5.46$ dB. Larger values of $R_G$ and $R_D$ improve the module's gain but also increase its reflection coefficients. However, increasing the drain resistance to $R_D = 300\ \Omega$ results in $|S_{22}| = 0.164$ (VSWR = 1.39 : 1) and improves the low frequency gain (17c) by approximately 1.3 dB to 6.78 dB. Choosing a characteristic impedance of $Z_{Gn} = Z_{Dn} = 125\ \Omega$, one calculates by employing (15a) an electrical length of $\theta_{G1} = \theta_{D1} = 27°$ for the shunt capacitance $C = C_{gs} = 0.25$ pF and the frequency $f = 20$ GHz. Using $C = C_{gs}$ to determine the line lengths provides a reasonable starting position for the amplifier's design, even though the input susceptance of the transistor is affected by other elements besides the gate–source capacitance. In contrast, for the determination

of the shunt capacitance $C_S$ in the drain line, it is appropriate to consider the influence of $C_{gs}$, $C_{dc}$, $C_{gd}$, and $C_{ds}$ on $C_S$. As initial design value we pick

$$C_S = \frac{C_{gs}}{1+\frac{C_{gd}}{C_{gs}}} - (C_{ds}+C_{dc}) = 0.159 \text{ pF}$$

to obtain reasonable circuit symmetry between gate and drain lines, and subsequently replace the capacitance $C_S$ = 0.159 pF with an open shunt stub of $Z_S = 50\ \Omega$. At the frequency $f = 20$ GHz, this requires an electrical length of $\theta_{Sn} = 45°$.

Starting with these parameters, i.e., $\theta_{G1} = \theta_{D1} = 27°$, $\theta_{G3} = \theta_{D2} = 13.5°$, $\theta_{S1} = \theta_{S2} = 45°$ (all at $f = 20$ GHz), $R_G = 50\ \Omega$, and $R_D = 300\ \Omega$, the gain and VSWR of the module are then optimized with the aid of a computer between 2 and 20 GHz, resulting in the element values presented in Table I and the performances plotted as curves *A* in Fig. 12. Table I also compares the values of the circuit elements before and after optimization. The comparison shows reasonably good proximity for the line lengths $\theta_{G1}$, $\theta_{G3}$, and $\theta_{D1}$. The termination of the idle gate port $R_G = 36\ \Omega$ in joint effort with the other elements brings about an improvement in gain flatness and especially in broad-band input VSWR. The input impedance transformer ($Z_T = 35\ \Omega$, $\theta_T = 32.3°$ at $f = 20$ GHz) was, as mentioned earlier, subjected to the amplifier's optimization together with all other elements listed in Table I.

### *B. Transmission Lines of Equal Electrical Lengths*

The uniform characteristic impedance approach requires curving of the drain line elements due to their longer lengths compared to the gate line elements. In this section we will show that a similar amplifier performance can be achieved with lines of different characteristic impedances and equal lengths between the active elements. The schematic of the "equal line lengths" approach is drawn in Fig. 11(b). This method makes it possible to place the GaAs MESFET's between two parallel straight lines making it a very simple structure. Based on experimental results, we found it to be beneficial for the performance of the amplifier to insert two line elements of different characteristic impedances between the transistors as shown in Fig. 11(b). In contrast to the "equal characteristic impedance circuit" of Fig. 11(a) which incorporates a one-element input matching circuit, we chose a two-element matching network for the "equal line lengths circuit." The computations of the amplifier's input and output parameters are again based on (5) employing the matrix (5a) and its submatrices (3a). Once the voltages and currents are known, the *S*-parameters of the amplifier can be determined. Gain and VSWR's versus frequency of the amplifier are plotted as curves *B* in Fig. 12. Except for a minor shift of the frequency band to higher frequencies, the characteristics of both amplifiers are very similar. Even though the equal characteristic impedance design has a slight performance advantage over the equal line lengths design, we chose the

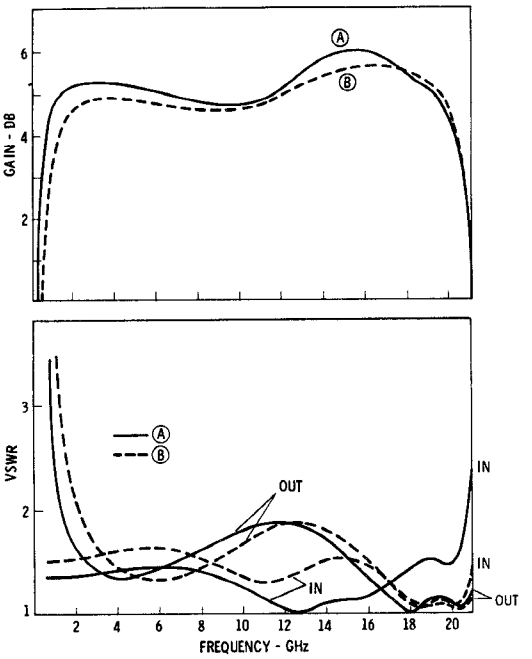


Fig. 12. Computed gain and VSWR of an optimized three-link distributed amplifier with transmission lines of equal characteristic impedances (curves *A*) or of equal electrical lengths (curves *B*).

TABLE I
ELEMENT VALUES OF THE MODULE WITH EQUAL CHARACTERISTIC IMPEDANCES BEFORE AND AFTER OPTIMIZATION

| ELEMENT | DIMENSION | BEFORE OPTIMIZATION | AFTER OPTIMIZATION |
|---|---|---|---|
| $\Theta_{G1}$ | DEGREES AT 20 GHz | 27.0 | 22.5 |
| $\Theta_{G3}$ | DEGREES AT 20 GHz | 13.5 | 14.9 |
| $\Theta_{D1}$ | DEGREES AT 20 GHz | 27.0 | 34.5 |
| $\Theta_{D2}$ | DEGREES AT 20 GHz | 13.5 | 4.9 |
| $\Theta_{S1}$ | DEGREES AT 20 GHz | 45.0 | 25.5 |
| $\Theta_{S2}$ | DEGREES AT 20 GHz | 45.0 | 0 |
| $R_G$ | OHM | 50 | 36 |
| $R_D$ | OHM | 300 | 300 |
| $L_D$ | nH | 10 | 9 |

($Z_{G1} = Z_{G2} = Z_{D1} = Z_{D2} = 125\ \Omega$; $Z_{S1} = Z_{S2} = 50\ \Omega$)

TABLE II
ELEMENT VALUES OF THE MODULE WITH EQUAL LINE LENGTHS

| | |
|---|---|
| $Z_{G1} = 65\ \Omega$ | $\Theta_{G1} = 12.2°$ |
| $Z_{G2} = 87\ \Omega$ | $\Theta_{G2} = 20.7°$ |
| $Z_{G3} = 87\ \Omega$ | $\Theta_{G3} = 15.2°$ |
| $Z_{D1} = 140\ \Omega$ | $\Theta_{D1} = 32.9°$ |
| $Z_{D2} = 140\ \Omega$ | $\Theta_{D2} = 6.7°$ |
| $R_G = 33\ \Omega$ | |
| $R_D = 400\ \Omega$ | |
| $L_D = 6$ nH | |

(DEGREES at 20 GHz)

latter for our practical amplifier module because of its simple layout. The electrical lengths between transistors for optimum performance are $\theta_{D1} = \theta_{G1} + \theta_{G2} = 32.9°$ at $f = 20$ GHz, while the corresponding characteristic impedances are $Z_{G1} = 65\ \Omega$, $Z_{G2} = 87\ \Omega$, and $Z_{D1} = 140\ \Omega$. All other circuit element values are listed in Table II. It should be pointed out that equal electrical lengths are not synonymous with equal physical lengths due to changes in the effective dielectric constant with line width. Depending on the dielectric substrate material, minor adjustments have to be made to the impedances of Table II when designing for equal physical lengths between the active devices.

## IV. Amplifier Fabrication and Performance

Of the two design techniques discussed in the previous chapter, the approach of equal line lengths was chosen for the design of our three-link amplifier module. Fused silica, 0.01 in in thickness, was used as substrate material for the input and output circuits. The choice of the material and its thickness was dictated by the high characteristic impedance of the drain line, and by the physical line lengths required between the transistors to accommodate the width of the source bias capacitors. Both the GaAs MESFET's and the bias capacitors were die-attached to a cooling rib located between the two substrates. The terminating resistors of the idle ports were etched into a tantalum nitride film which was deposited below the substrates' thin gold film. The overall dimension of the module's circuit are $0.2 \times 0.176$ in. Biasing created somewhat of a problem due to the unit's ultra-wide bandwidth. Since it was decided to attach the drain potential directly to the drain line by means of a high-impedance line rather than passing the drain current through the terminating resistor, the amplifier's output match was compromised. As a result, however, a significant power dissipation (1.35 W) in the drain resistor $R_D$ was avoided.

The measured small-signal gain, reverse isolation, and return loss of the three-link amplifier module whose idle ports were terminated with $R_G = 38\ \Omega$ and $R_D = 125\ \Omega$ are plotted in Fig. 13. Over the frequency band of 2–20 GHz, a small signal gain of $5.5 \pm 0.6$ dB and a minimum reverse isolation of 22 dB were measured. The maximum VSWR's over the 10:1 bandwidth were 2.2:1 for the input and 2.5:1 for the output port. As pointed out earlier, the output match was compromised by connecting the drain bias circuit directly to the drain line. Also shown in Fig. 13 are the theoretical curves for small-signal gain, reverse isolation, and return loss. They have been computed for the schematic of Fig. 11(b) and the GaAs MESFET model of Fig. 9 with the following exceptions: $R_G = 38\ \Omega$, $R_D = 125\ \Omega$, and $g_m = 28$ mS. In addition, the inductivity $L_D$ of Fig. 11(b) was replaced by a short-circuit shunt stub of $Z = 200\ \Omega$ and $L = 0.185$ in. These changes represent the actual values measured on the amplifier. The reduction of the drain resistor $R_D$ from the computed value of 400 Ω to the applied value of 125 Ω was made because it improved the module's gain flatness and output match when employing the $g_m = 28$-mS transistor. A comparison between the measured and computed curves of the small-signal gain shows excellent agreement. The same is true for the reverse isolation. Considering the wide bandwidth, the agreement between computed and measured return loss, especially for the input port, came out much better than expected. Initial power measurements resulted in a minimum output power of 19.3 dBm at the 1-dB compression points between 2 and 18 GHz. For these measurements, the amplifier was operated at $V_{DS} = 6$ V and $I_{DS} = 117$ mA. No attempt was made to tune for optimum output power.

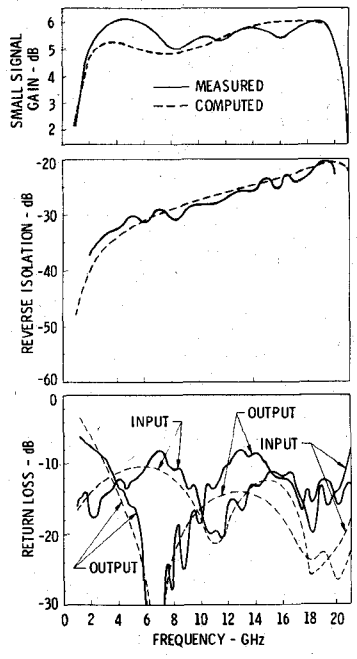


Fig. 13. Measured and computed small-signal gain, reverse isolation, and return loss of a three-link distributed amplifier. ($V_{DS} = 4$ V, $V_{GS} = -0.7$ V and $I_{DS} = 104$ mA.)

## V. Conclusion

Formulas to calculate the *S*-parameters of distributed amplifiers consisting of lumped circuit elements or distributed line elements have been developed. They were initially evaluated for a simplified transistor model made up of three elements. While contributing to the understanding of the distributed amplifier's operation, the formulas' quantitative predictions of gain are only fair. For this reason, the analysis was extended to amplifiers whose transistors are represented by *S*-parameter derived models resulting in accurate predictions of the amplifiers' gain and VSWR performance. At first the case of identical circuit elements in both the gate and the drain line with the idle ports terminated by 50-Ω impedances was analyzed. Subsequent studies were concerned with the more general case of unequal circuit elements and arbitrary termination impedances of the idle ports. Finally, all circuit element parameters, as well as the impedances terminating the idle ports, were subjected to performance optimization. As a result, the amplifier concept of equal characteristic impedances and that of equal line lengths were introduced. Formulas for the *S*-parameters were presented that characterize the performance of the distributed amplifier at low frequen-

cies. However, computed results show that the gain determined with these formulas can be maintained up to $f = 20$ GHz for the GaAs MESFET module employed. Even though the concepts of equal characteristic impedances and equal line lengths are basically equivalent in overall performance, the latter was chosen for the final design of a three-link amplifier due to practical reasons. Comparisons between measured and computed results show excellent agreement in case of the small-signal gain and the reverse isolation and reasonable agreement in case of the return loss. In addition, measurements reveal the principle's ultra-broad-band power handling capabilities.

## ACKNOWLEDGMENT

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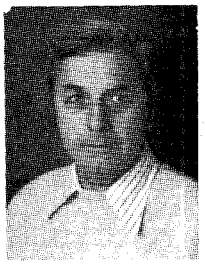

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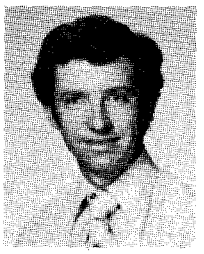
Dr. Niclas received the outstanding publications award in 1962 of the German Society of Radio Engineers.



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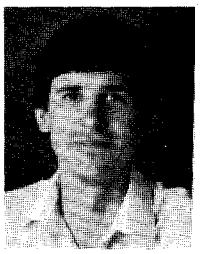

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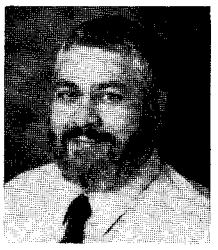

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